PCB Layout and Design Considerations for the CH7305 Single/Dual LVDS Transmitter

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7305 Single/Dual LVDS Transmitter. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for the LVDS output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures shown in this document are based on the 64-pin LQFP package of the CH7305 designed with an Intel Brookdale® / Intel Springdale® system.

2. Component Placement

Components associated with the CH7305 encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7305 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7305 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7305 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage VDDV), and PLL power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment

Pin #	# of pins	Type	Symbol	Description
42, 64	2	Power	DVDD	Digital Supply Voltage (3.3V)
35, 49	2	Power	DGND	Digital Ground
48	1	Power	VDDV	I/O Supply Voltage (1.1V to 3.3V)
5, 11, 22, 28	4	Power	LVDD	LVDS Supply Voltage (3.3V)
8, 14, 19, 25, 31	5	Power	LGND	LVDS Ground
38	1	Power	LPLL_VDD	LVDS PLL Supply Voltage (3.3V)
36	1	Power	LPLL_GND	LVDS PLL Ground

- **Digital and PLL Power Pins Decoupling and Connection**

  Figure 1 shows the decoupling and connection for the LPLL_VDD, LVDD, and DVDD.

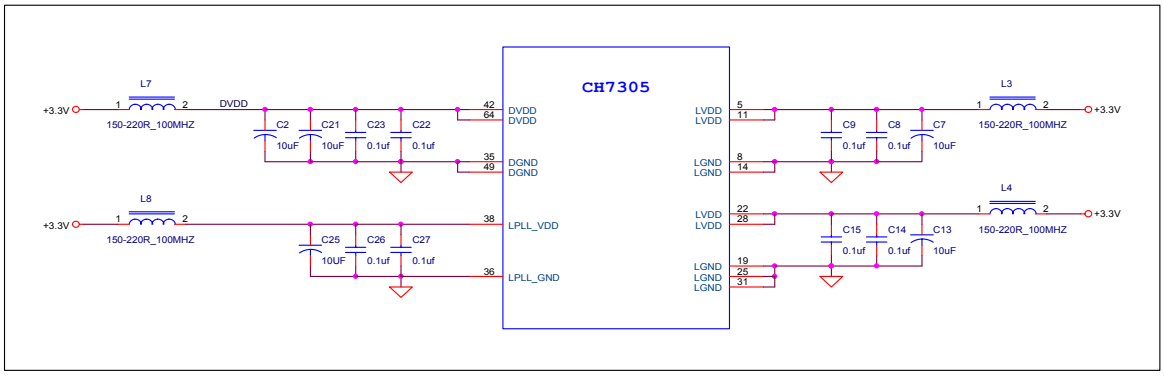


Figure 1: Digital and PLL Power pins Decoupling and Connection

Note: All the Ferrite Beads described in this document are recommended to have <.05 Ω at DC; 2 3Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for detail or an equivalent part can be used for the diagram.

- **VDDV and VREF Decoupling and Connection**

  VDDV is the I/O supply voltage. This pin should be decoupled and connected to the maximum voltage level seen by the I/O of the CH7305 (1.1V to 3.3V).

  VREF inputs a reference voltage of VDDV/2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, syncs and clock inputs. Please refer to **Figure 2** for the decoupling and connection.

  Figure 2 shows the decoupling and connection for VDDV, and VREF.

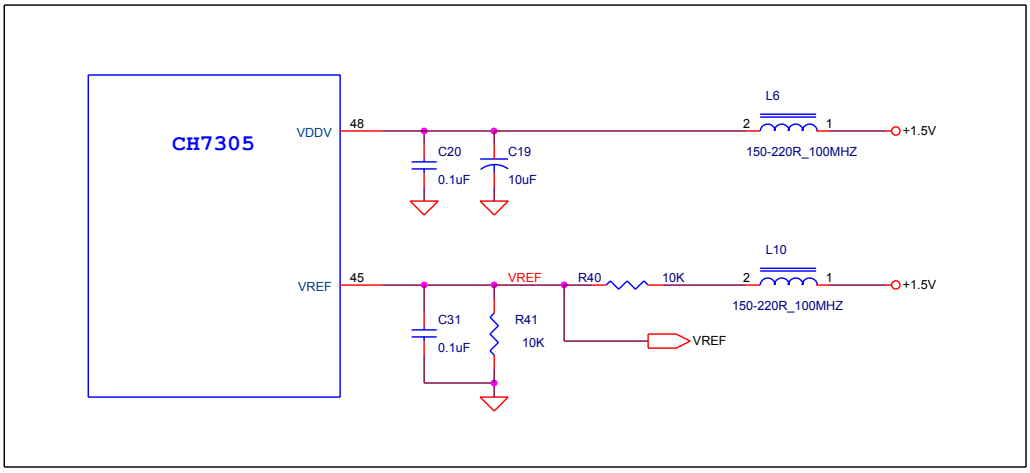


Figure 2: VDDV and VREF pins Decoupling and Connection

2.2 General Control

- **GPIO pin**

  This pin provides a general purpose I/O and is controlled via the serial port. The direction of the signal is controlled by register 1Eh, GPIO Direction Control Register. When the direction is set as "input", the GPIO pin has a weak pull-up (about 1 MΩ). See **Figure 3** for design reference. In the reference design, the GPIO pin is connected with a pair of resistors, which allow the designer to either pull up or pull down the pin. If it should be set to HIGH, R65 can be stuffed with a 10 KΩ resistor, and R66 should not be stuffed. If it is to be set to LOW, then R65 should be not stuffed, and R66 can be stuffed with a 330Ω resistor.

- **RESET* pin**

  RESET* pin, which is internal pull-up, When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port. In the reference design, this pin is connected to the RST* pin of Intel's DVO port.

- **LPLL_CAP pin**

  The LPLL_CAP pin allows coupling of any signal to the on-chip loop filter capacitor. A capacitor with a typical value of 0.1 nF, should be connected between this pin (pin 37) and ground (See **Figure 3**).

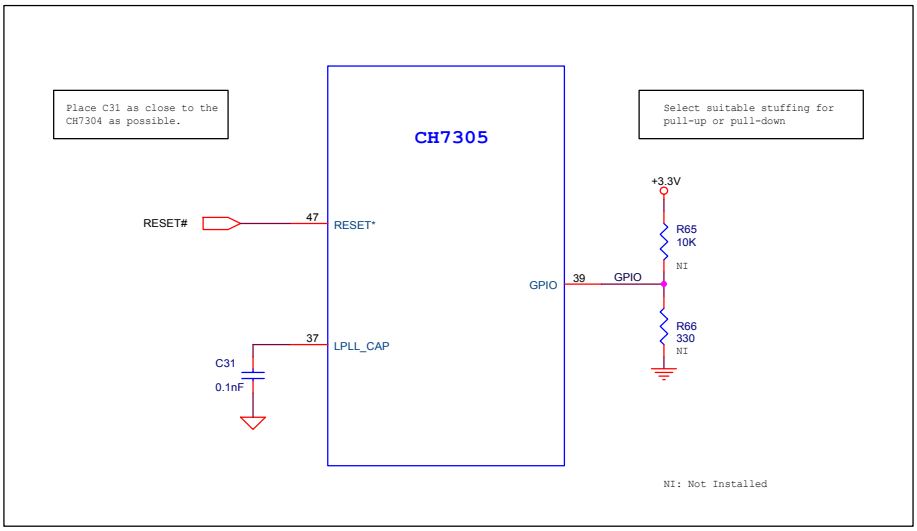


Figure 3: General Control Reference Design

2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

  Crystal Input

  The 14.31818 MHz crystal must be placed as close as possible to the XI and XO pins (pins 34 and 33), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7305 encoder, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent to these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7305 pin 35 ground.

Reference Crystal Oscillator

The CH7305 includes an oscillator circuit which allows a 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7305. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be 14.31818 MHz and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to the CH7305 (C_{ext}).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$\mathbf{C_{ext} = (2 \times C_L) - C_{int} - 2C_S}$$

where:

C_{ext}= external load capacitance required on XI and XO pins.

C_L= crystal load capacitance specified by crystal manufacturer.

C_{int}= capacitance internal to CH7305 (approximately 10-15 pF on each of XI and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 4** for the symbols used in the calculation described above.

In general, let us assume

C_{int} XI = C_{int} XO = C_{int}

C_{ext} XI = C_{ext} XO = C_{ext}

such that

$C_L = (C_{int} + C\ ext) / 2 + C_S$ and $C\ ext = 2 (C_L - C_S) - C_{int}$

$= 2\ C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int}/2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to AN-06.

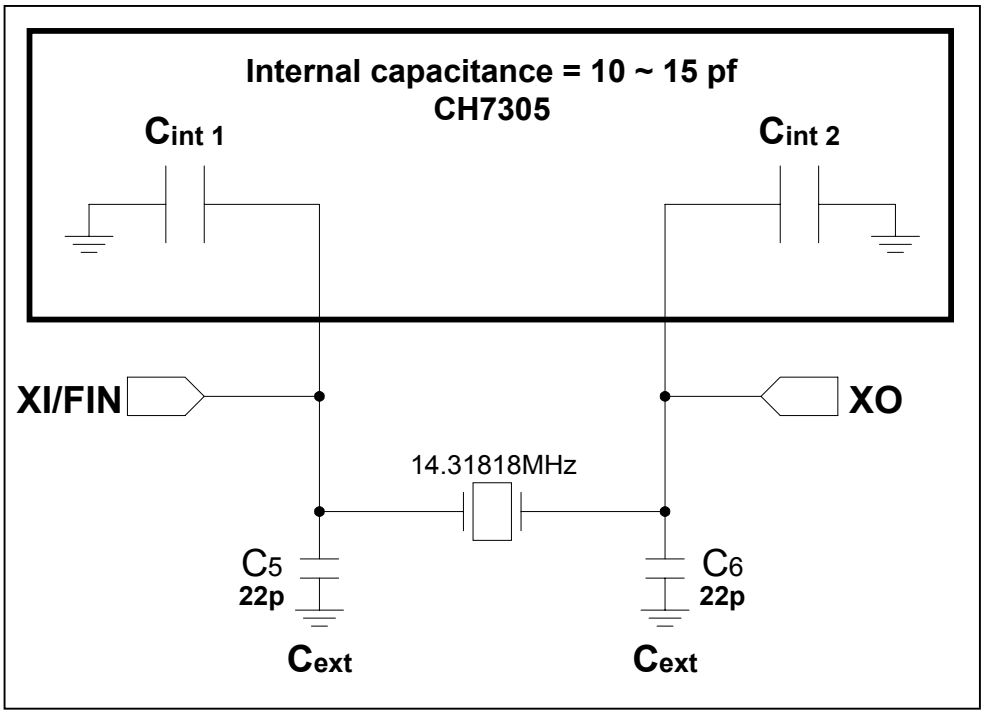


Figure 4: Reference Crystal Design.

- **XCLK, XCLK* (External Clock Input) pins**

  XCLK and XCLK* form a differential clock signal input to CH7305 for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. In the reference design these pins are connected to DVOC_CLK and DVOC_CLK# (see **Figure 5** for reference design).

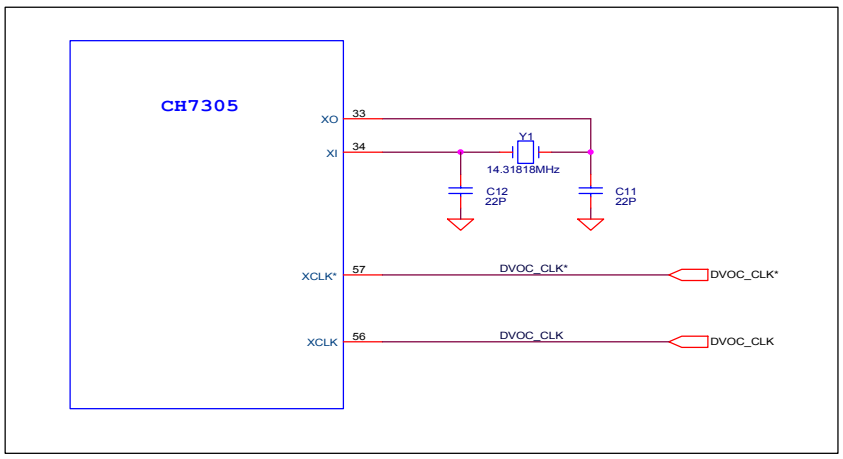


Figure 5: Clock and Crystal Oscillator Reference Design

2.4 Serial Ports Control

- **SPD and SPC pins**

  SPD (pin 41) and SPC (pin 40) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 2.2 KΩ resistors.

  The Device Address Byte of the CH7305 is defined as {1 1 1 0 1 0 1 R/W}. For serial port writes, the Device Address Byte is EAh and for serial port reads, the Device Address Byte is EBh.

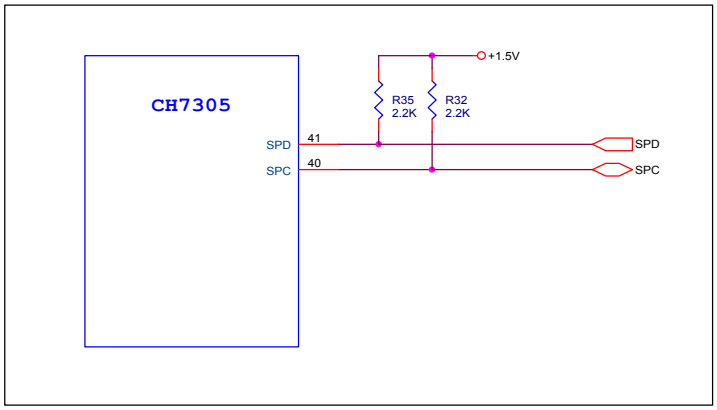


Figure 6: Serial Port Control Reference Design

2.5 Data Input and Syncs

Since the digital pixel data and the pixel clock of the CH7305 may toggle at speeds of up to 165MHz (depending on the input mode), it is critical that the connection of these video input signals between the graphics controller and the CH7305 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

- **D[11:0]**

  These data pins accept a set of 12 data inputs from a digital video port of a graphics controller. The levels are from 0 to VDDV. VREF is the threshold level. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used when routing these signals.

- **H and V**

  These pins accept horizontal/vertical sync inputs for use with the D[11:0] input data. The amplitude will be 0 to VDDV. VREF is the threshold level for these inputs.

Figure 7 shows the reference design example for data input and syncs.

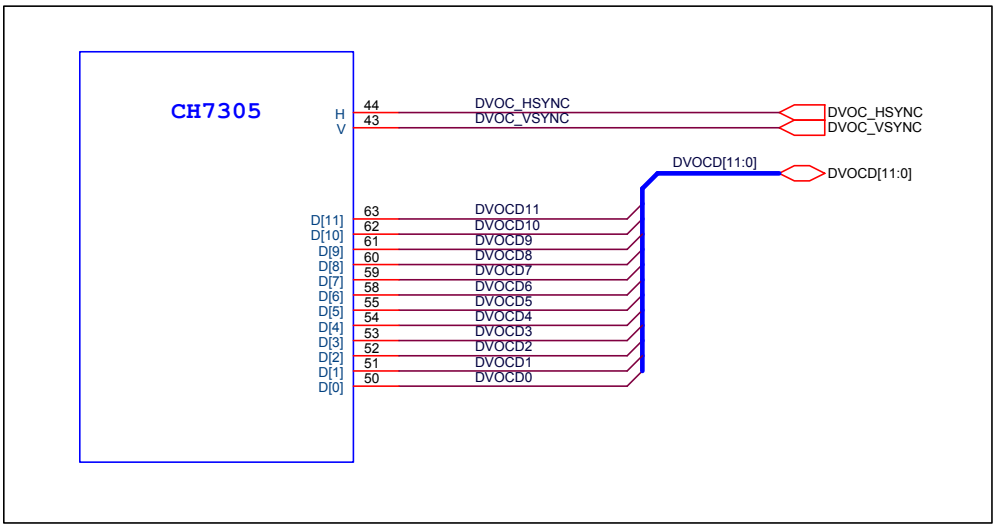


Figure 7: Data Input and Syncs Reference Design

2.6 LVDS Output and Control

The LVDS output pins include: LDC[7:0], LL1C, LL1C*, LL2C, LL2C*. The LVDS control pins include: VSWING, DE, ENAVDD, and ENABKL. The connection of these pins are described as follows. **Figure 8** shows a reference design example for LVDS output and control.

- **VSWING**

  VSWING is the LVDS swing control. This pin sets the swing level of the LVDS outputs. A 2.4 KΩ resistor should be connected between this pin and LGND (pin 35) using short and wide traces.

- **DE**

  DE is the Data Enable control pin.

  This pin accepts a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are from 0 to VDDV. VREF is the threshold level.

- **ENAVDD, ENABKL**

  ENAVDD (pin 2) and ENABKL (pin 1) are for LVDS panel power control: ENAVDD enables the panel's 3.3V VDD and ENABKL enables the panel's back-light. In the reference design, these pins are connected to the panel's VDD and backlight control circuits respectively.

- **LDC[7:0], LLC1, LLC1*, LLC2, LLC2***

  The LDC[7:0], LL1C, LL1C*, LL2C, LL2C* signals are high frequency differential signals that need to be routed with special precautions. They must be routed in pairs with the length as close as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the connector without any vias to the bottom layer. Trace for the LVDS signals should be closely coupled and the trace should be 100Ω differential impedance (50Ω to the ground from each differential pin).

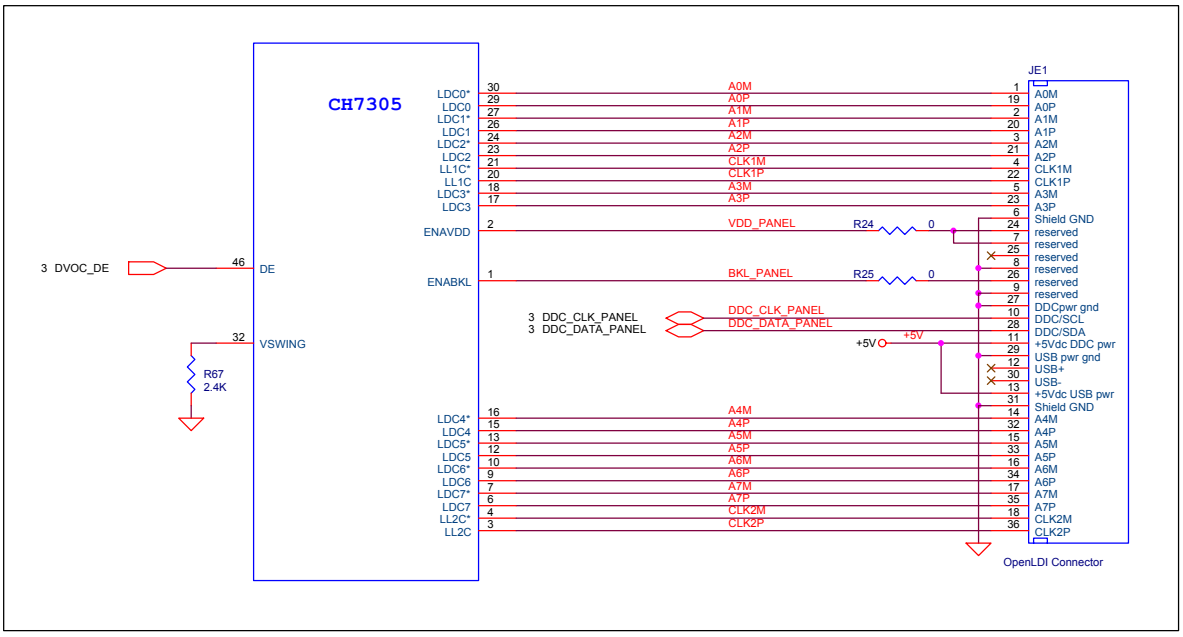


Figure 8: LVDS Output and Control Reference Design

3. LVDS Output Design Tips

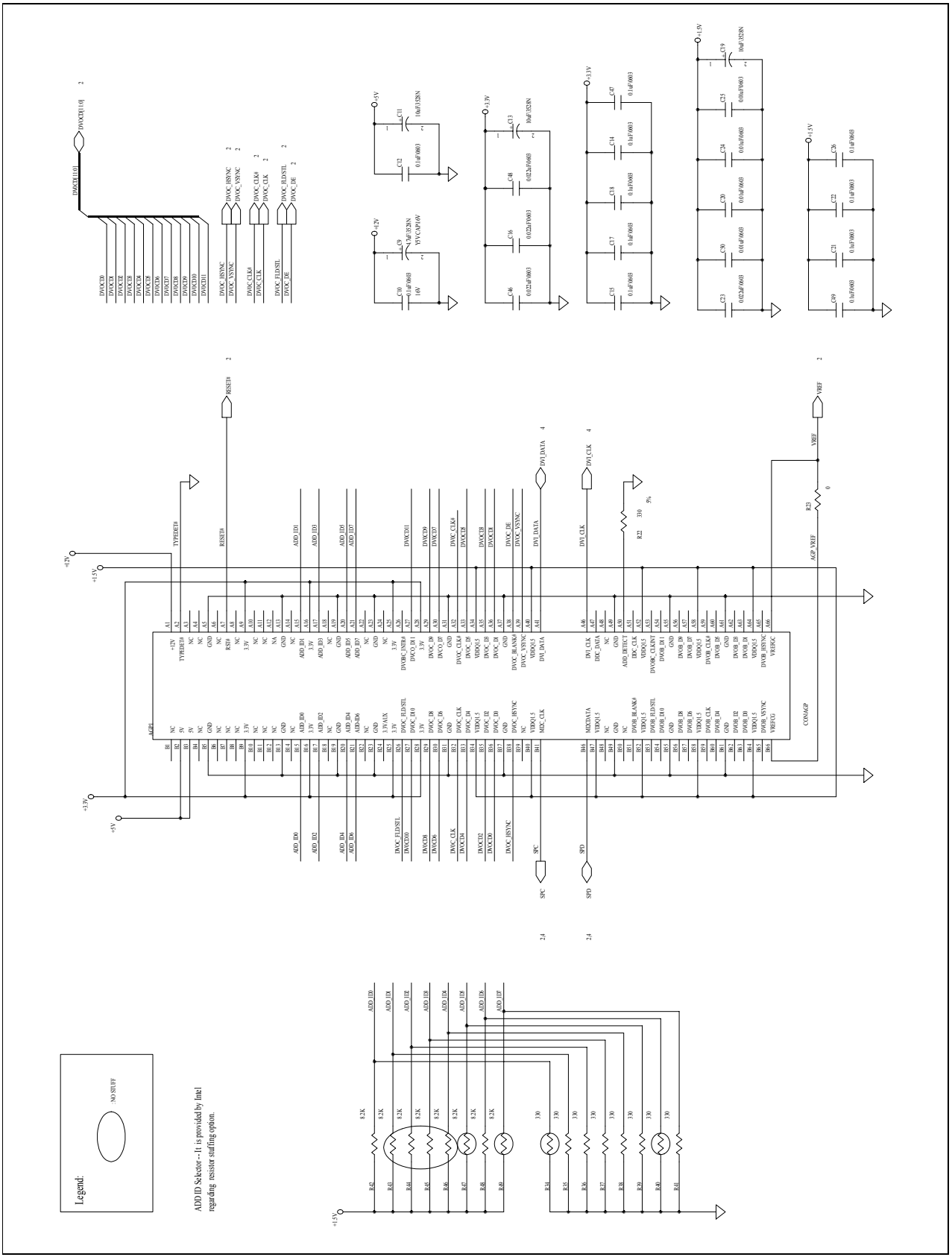
Output and Control Reference Design

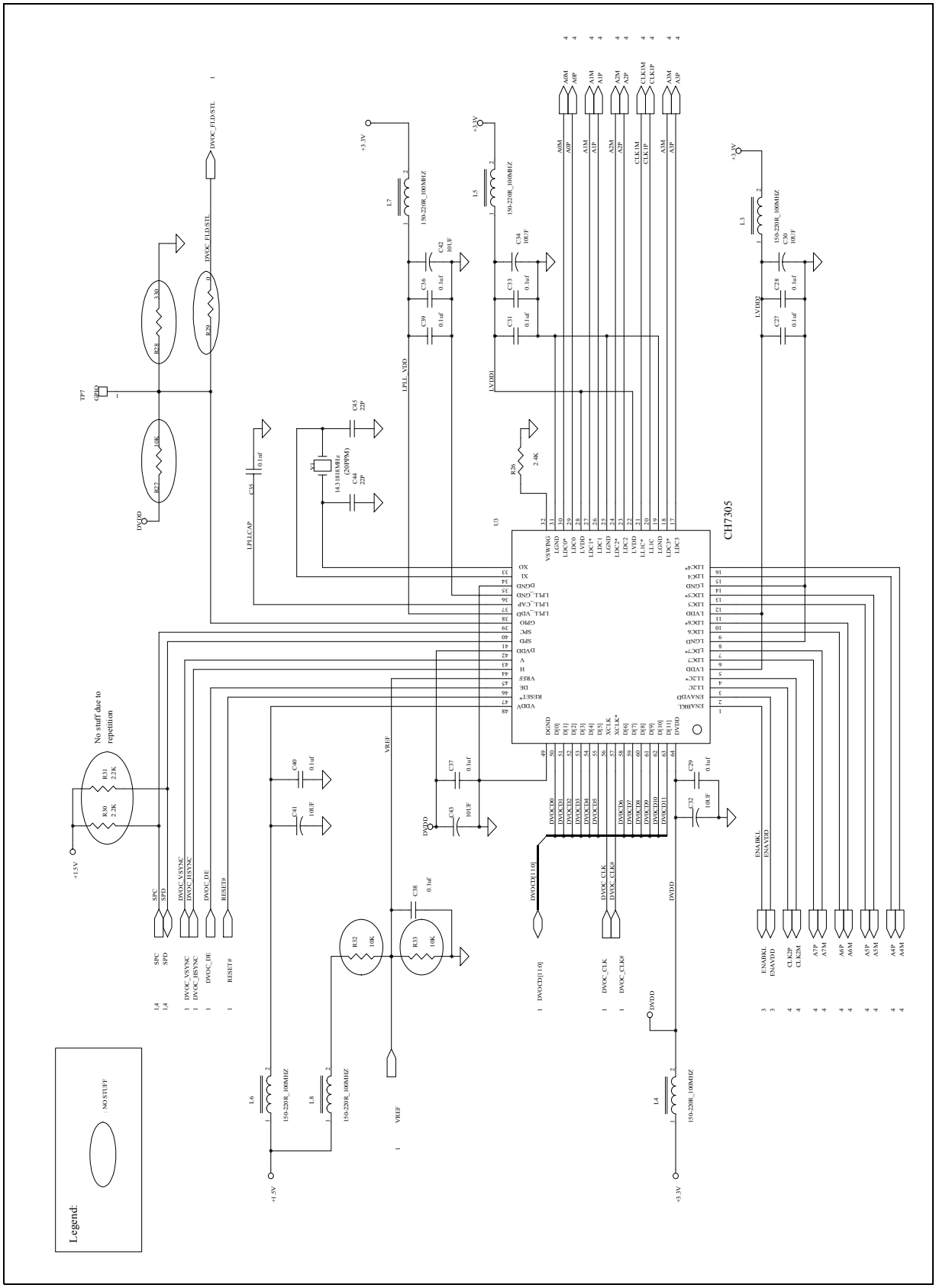
- Dedicating planes for Vcc and Ground are typically required for high-speed design. The solid ground plane is required to establish a controlled impedance for the transmission line interconnects. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance.
- If it is possible, put CMOS/TTL signals and LVDS signals on a different layers which should be isolated by the power and ground planes.
- Power and ground should use wide (low impedance) traces. Do not use 50Ω design rules on power and ground traces.
- Keep ground PCB return paths short and wide. Provide a return path that creates the smallest loop for the image currents to return.
- Traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance. This not only reduces EMI, but also helps to ensure noise coupled onto the conductors will be common-mode noise.
- Leave all unused LVDS and CMOS/TTL output open. Do not tie them to ground.
- Tie unused transmitter inputs and control/enable signals to power or ground using pull-up or a pull-down resistors.

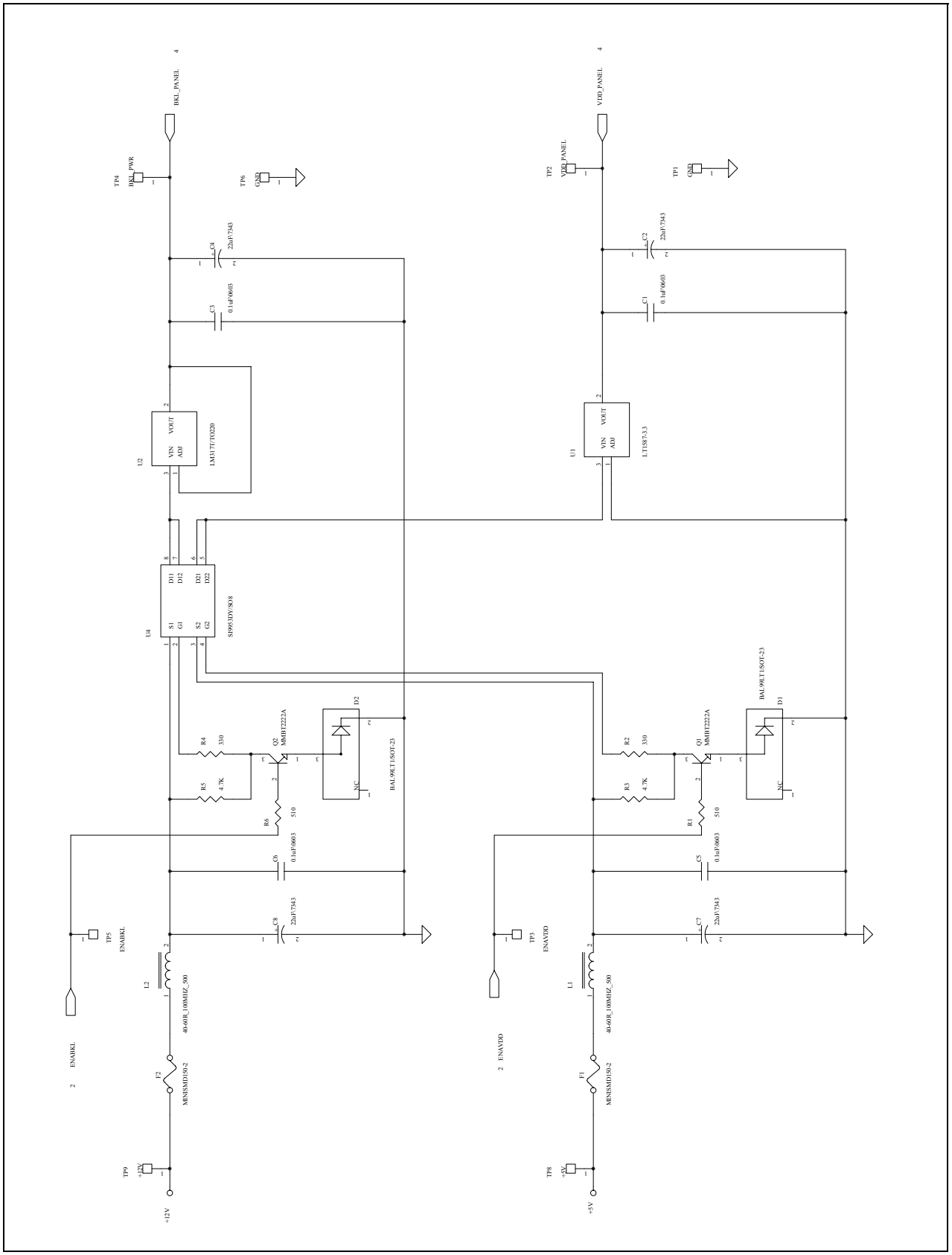
4. Reference Design Example

The following schematic are given to be used as a CH7305 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7305 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

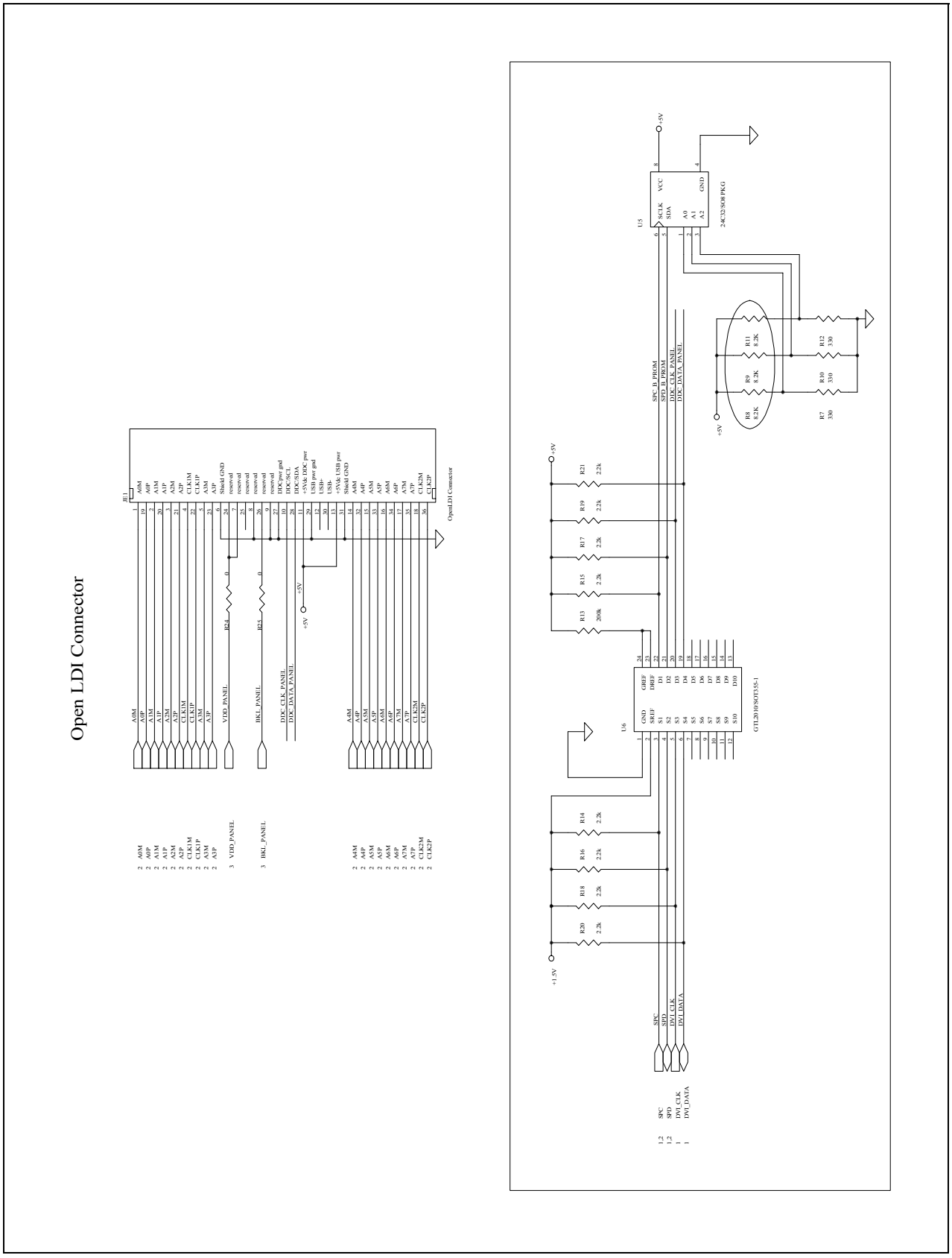
4.1 Schematics of Reference Design Example


Legend:
NO STUFF
ADD ID Selector - U1 is provided by Intel regarding resistor stuffing option.


CH7305
U3
DVOC_FLD/STL
DVOC_VSYNC
DVOC_HSYNC
DVOC_DE
RESET#
SPC
SPD
DVOCD[11:0]
DVOC_CLK
DVOC_CLK#
VREF
LPLL_VDD
LVDD1
LVDD2
DVDD
ENABKL
ENAVDD
CLK1M
CLK1P
A0M
A0P
A1M
A1P
A2M
A2P
A3M
A3P
A4M
A4P
A5M
A5P
A6M
A6P
CLK2M
CLK2P
ATM
ATP
No stuff due to repetition
Legend:
NO STUFF


BKL_PANEL
VDD_PANEL
TP4 BKL_PWR
TP6 GND
TP2 VDD_PANEL
TP1 GND
C4 22uF/7343
C3 0.1uF/0603
C2 22uF/7343
C1 0.1uF/0603
U2 LM317T/TO220
U1 LT1587-3.3
U4 SI9953DY/8038
D2 BAL99LT1/SOT-23
D1 BAL99LT1/SOT-23
Q2 MMBT2222A
Q1 MMBT2222A
R4 330
R5 4.7K
R6 510
R2 330
R3 4.7K
R1 510
C6 0.1uF/0603
C5 0.1uF/0603
C8 22uF/7343
C7 22uF/7343
TP5 ENABKL
TP3 ENAVDD
L2 40/40R_100MHZ_500
L1 40/40R_100MHZ_500
F2 MINISMD150-2
F1 MINISMD150-2
TP9 +12V
TP8 +5V
+12V
+5V
ENABKL
ENAVDD

Open LDI Connector



5. Revision History

Rev. #	Date	Section	Description
1.0	2/12/03	All	First official release.

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